20 standard cubic centimeters per minute (sccm); and (6) an argon flow rate of from about 100 to about 300 standard cubic centimeters per minute (sccm), for a time period sufficient to completely etch through the blanket hard mask layer **38** when forming the patterned hard mask layers **38***a*, **38***b* and **38***c*.

Referring now to FIG. **6**, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronics fabrication whose schematic cross-sectional diagram is illustrated in FIG. **5**. Shown in FIG. **6** is a schematic cross-sectional diagram of a microelectronics fabrication otherwise equivalent to the microelectronics fabrication whose schematic cross-sectional diagram is illustrated in FIG. **5**, but wherein there has been simultaneously: (1) stripped from the patterned hard mask layers **38***a*, **38***b* and **38***c* the corresponding patterned photoresist layers **40***a*, **40***b* and **40***c*; and (2) patterned the blanket inter-metal dielectric (IMD) layer **36** to form the patterned inter-metal dielectric (IMD) layers **36***a*, **36***b* and **36***c*, through etching with a second etching plasma **44**. Within the second preferred embodiment of the present invention, the second etching plasma **44** is preferably employs methods and materials analogous or equivalent to the methods and materials employed in forming the second etching plasma **20** within the first preferred embodiment of the present invention as illustrated within the schematic cross-sectional diagram of FIG. **3**.

More preferably, the second etching plasma **44** is employed within a oxygen containing plasma etch method which employs an oxygen and argon containing etchant gas composition. Preferably, the oxygen containing plasma etch method also employs: (1) a reactor chamber pressure of from about 2 to about 10 mtorr; (2) a source radio frequency power of from about 500 to about 1500 watts at a source radio frequency of 13.56 MHZ; (3) a bias radio frequency power of from about 1000 to about 2000 watts; (4) an oxygen flow rate of from about 10 to about 50 standard cubic centimeters per minute (sccm); and (5) an argon flow rate of from about 5 to about 20 standard cubic centimeters per minute (sccm), for a time period sufficient to reach the patterned conductor layers **34***a* and **34***b*, while simultaneously forming the patterned inter-metal dielectric (IMD) layers **36***a*, **36***b* and **36***c*. Optionally, there may also be employed within the second etching plasma **44** a helium background gas at a flow of from about 1 to about 5 standard cubic centimeters per minute (sccm) and/or a hexafluoroethane etchant gas at a flow of from about 1 to about 5 standard cubic centimeters per minute (sccm).

When employing within the second preferred embodiment of the present invention the preferred materials as disclosed above for the patterned photoresist layers **40***a*, **40***b* and **40***c*, the blanket hard mask layer **38** and the blanket inter-metal dielectric (IMD) layer **36**, along with the methods and materials as disclosed within the first etching plasma **42** and the second etching plasma **44**, there is formed the microelectronics fabrication as illustrated within FIG. **6**. The microelectronics fabrication has formed therein a pair of interconnection vias through an inter-metal dielectric layer accessing a pair of patterned conductor layers, where the pair of interconnection vias is formed with attenuated lateral etching of the pair of interconnection vias when stripping from a series of patterned hard mask layers a series of patterned photoresist layers employed in defining the pair of vias through the inter-metal dielectric (IMD) layer.

As is understood by a person skilled in the art, various of the embodiments of microelectronics fabrications as disclosed by Havemann, in U.S. Pat. No. 5,565,384, the teachings of which are incorporated herein fully by reference, may also be modified in accord with the method of the present invention as disclosed herein.

As is similarly understood by a person skilled in the art, the preferred embodiments of the present invention are illustrative of the present invention rather than limiting of the present invention. Revisions and modifications may be made to methods, materials, structures and dimensions through which are fabricated microelectronics fabrications in accord with the preferred embodiments of the present invention while still providing embodiments which are within the spirit and scope of the present invention, as defined by the appended claims.

What is claimed is:

1. A method for forming a patterned microelectronics layer within a microelectronics fabrication comprising:

providing a substrate employed within a microelectronics fabrication;

forming over the substrate an oxygen containing plasma etchable microelectronics layer;

forming upon the oxygen containing plasma etchable microelectronics layer a hard mask layer;

forming upon the hard mask layer a patterned photoresist layer;

etching through use of a first anisotropic plasma etch method the hard mask layer to form a patterned hard mask layer while employing the patterned photoresist layer as a first etch mask layer, the first anisotropic plasma etch method employing an etchant gas composition appropriate for etching a hard mask material from which is formed the hard mask layer;

etching through use of a second plasma etch method the patterned photoresist layer from the patterned hard mask layer while employing the patterned hard mask layer as an etch stop layer while simultaneously etching the oxygen containing plasma etchable microelectronics layer while employing at least the patterned hard mask layer as a second etch mask layer to form a patterned oxygen containing plasma etchable microelectronics layer, the second plasma etch method employing an oxygen containing etchant gas composition.

2. The method of claim **1** wherein a thickness of the patterned photoresist layer and a thickness of the oxygen containing plasma etchable microelectronics layer are each selected to provide that:

the patterned photoresist layer is completely etched from the patterned hard mask layer;

the oxygen containing plasma etchable microelectronics layer is completely etched to form the patterned oxygen containing plasma etchable microelectronics layer; and

there is attenuated lateral etching of the patterned oxygen containing plasma etchable microelectronics layer.

3. The method of claim **1** wherein the microelectronics fabrication is selected from the group consisting of integrated circuit microelectronics fabrications, solar cell microelectronics fabrications, ceramic substrate microelectronics fabrications and flat panel display microelectronics fabrications.

4. The method of claim **1** wherein the oxygen containing plasma etchable microelectronics layer is formed from an oxygen containing plasma etchable material selected from the group consisting of oxygen containing plasma etchable conductor materials, oxygen containing plasma etchable semiconductor materials and oxygen containing plasma etchable dielectric materials.

5. The method of claim 1 wherein the hard mask layer is formed from a hard mask material selected from the group consisting of metals, metal alloys, metal oxides, metal nitrides, non-metal oxides, non-metal nitrides and composites thereof.

6. The method of claim 1 wherein the oxygen containing etchant gas composition employs an oxygen containing etchant gas selected from the group consisting of oxygen, ozone, nitrous oxide and nitric oxide.

7. The method of claim 6 wherein the oxygen containing etchant gas composition also employs a sputtering gas component.

8. A microelectronics fabrication having formed therein a patterned oxygen containing plasma etchable microelectronics layer formed in accord with the method of claim 1.

9. A method for forming a patterned microelectronics dielectric layer within a microelectronics fabrication comprising:

providing a substrate employed within a microelectronics fabrication;

forming over the substrate an oxygen containing plasma etchable microelectronics dielectric layer;

forming upon the oxygen containing plasma etchable microelectronics dielectric layer a hard mask layer;

forming upon the hard mask layer a patterned photoresist layer;

etching through use of a first anisotropic plasma etch method the hard mask layer to form a patterned hard mask layer while employing the patterned photoresist layer as a first etch mask layer, the first anisotropic plasma etch method employing an etchant gas composition appropriate for etching a hard mask material from which is formed the hard mask layer;

etching through use of a second plasma etch method the patterned photoresist layer from the patterned hard mask layer while employing the patterned hard mask layer as an etch stop layer while simultaneously etching the oxygen containing plasma etchable microelectronics dielectric layer while employing at least the patterned hard mask layer as a second etch mask layer to form a patterned oxygen containing plasma etchable microelectronics dielectric layer, the second plasma etch method employing an oxygen containing etchant gas composition.

10. The method of claim 9 wherein a thickness of the patterned photoresist layer and a thickness of the oxygen containing plasma etchable microelectronics dielectric layer are each selected to provide that:

the patterned photoresist layer is completely etched from the patterned hard mask layer;

the oxygen containing plasma etchable microelectronics dielectric layer is completely etched to form the patterned oxygen containing plasma etchable microelectronics dielectric layer; and

there is attenuated lateral etching of the patterned oxygen containing plasma etchable microelectronics dielectric layer.

11. The method of claim 9 wherein the microelectronics fabrication is selected from the group consisting of integrated circuit microelectronics fabrications, solar cell microelectronics fabrications, ceramic substrate microelectronics fabrications and flat panel display microelectronics fabrications.

12. The method of claim 9 wherein the oxygen containing plasma etchable microelectronics dielectric layer is formed from an oxygen containing plasma etchable dielectric material selected from the group consisting of organic polymer spin-on-polymer dielectric materials and amorphous carbon dielectric materials.

13. The method of claim 9 wherein the hard mask layer is formed from a hard mask material selected from the group consisting of silicon oxide hard mask materials, silicon nitride hard mask materials and silicon oxynitride hard mask materials.

14. The method of claim 9 wherein the oxygen containing etchant gas composition employs an oxygen containing etchant gas selected from the group consisting of oxygen, ozone, nitrous oxide and nitric oxide.

15. The method of claim 14 wherein the oxygen containing etchant gas composition also employs a sputtering gas component.

16. A microelectronics fabrication having formed therein a patterned oxygen containing plasma etchable microelectronics dielectric layer in accord with the method of claim 9.

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